In the claims

Please amend the claims as follows:

1. to 14. (cancelled)

15. (new) An asynchronous transfer mode (ATM) communications system, comprising:

a packet scheduler including:

a packet scheduler processor for scheduling assembly of real-time, delay sensitive traffic data into ATM packets of an ATM bearer virtual circuit connection (VCC);

an assembly processor for assembling said real-time, delay sensitive traffic data into the ATM packets of said bearer VCC under the control of the packet scheduler processor; and

a control processor for controlling dispatch of the ATM packets in conformance with a traffic characteristic of said bearer VCC;

wherein said packet scheduler processor has a timer having a pre-set holdover timing period which is reset at the start of each ATM packet assembly process, whereby, if the holdover timing period expires prior to complete assembly of an ATM packet, then, on expiry of said holdover timing period, the packet scheduler dispatches the partially filled ATM packet.

16. (new) A communications system as claimed in claim 15, wherein the packet scheduler processor has a minimum inter-cell period timer which has a pre-set timing period (Tmin) which is reset at the start of each ATM packet assembly process whereby, if assembly of an ATM packet is completed prior to expiry of the inter-cell timing period, then the packet scheduler does not dispatch said ATM packet until after expiry of said timing period (Tmin), and wherein said timing period (Tmin) is set such that it obeys the relationship:

Tmin ≤ holdover timing period.

17. (new) A communications system as claimed in claim 16, wherein the inter-cell timing period (Tmin) defines said traffic characteristic of the bearer VCC.

18. (new) A communications system as claimed in claim 17, wherein the inter-cell timing period (Tmin) is a function of the permissible peak cell rate (PCR) of the bearer VCC.

19. (new) A communications system as claimed in claim 18, wherein the inter-cell timing period (Tmin) is set to be equal to the reciprocal of the PCR of the bearer VCC, namely Tmin = 1/PCR.

20. (new) A communications system as claimed in claim 16, wherein the packet scheduler processor has a sustained inter-cell timing period timer having a pre-set time period (Tsus) which is set such that it obeys the relationship:

Tmin ≤ Tsus ≤ holdover timing period.

21. (new) A communications system as claimed in claim 20, wherein the Tsus and Tmin timing periods together define the traffic characteristic of the bearer VCC.

22. (new) A communications system as claimed in claim 21, wherein the sustained inter-cell timing period (Tsus) is a function of the permissible sustained cell rate (SCR) of the bearer VCC.

23. (new) A communications system as claimed in claim 22, wherein the Tsus timing period is set to be equal to the reciprocal of the SCR, namely Tsus= 1/SCR.

24. (new) A communications system as claimed in claim 21, wherein, in addition to controlling dispatch of the ATM packets in conformance with a traffic characteristic of the bearer VCC defined by both the Tmin and Tsus timing periods, the control processor is arranged to control dispatch of the ATM packets on said bearer VCC in accordance with a burst tolerance (BT) characteristic which is determined from the relationship:

$$BT = (MBS-1).(1/SCR-1/PCR)$$

where MBS is the maximum packet burst size permissible on the bearer VCC.

25. (new) A communications system as claimed in any one of claims 15 to 24, wherein the assembly processor performs a multiplexing function to multiplex ATM common part sublayer payload data units (CPS-PDUs) assembled from ATM adaptation layer 2 mini-cells encapsulating the real-time, delay sensitive traffic data into the ATM packets for dispatch on the bearer VCC.

26. (new) A communications system as claimed in claim 15, wherein the control processor is arranged to configure parameters for controlling operation of the packet scheduler and wherein the system includes a packet scheduler parameter store for storing the parameters configured by the control processor.

27. (new) A communications system as claimed in claim 26, wherein the control processor is arranged to modify the parameters for controlling operation of the packet scheduler during a lifetime of the bearer VCC.

28. (new) A communications system as claimed in claim 26, wherein the control processor is arranged to configure initial status parameters for a new bearer VCC, said status parameters controlling the packet scheduling process and wherein the system includes a VCC scheduler status store for maintaining the configured VCC initial status parameters.

29. (new) A communications system as claimed in claim 25, wherein the system includes an incoming packet processor for receiving AAL2 mini-cells encapsulating said real-time, delay sensitive traffic data and wherein said incoming packet processor determines an outgoing bearer VCC for each received mini-cell.

30. (new) A communications system as claimed in claim 29, wherein the incoming packet processor determines a priority for each received mini-cell.

31. (new) A communications system as claimed in claim 29, wherein the system includes a dynamic buffer for queuing received mini-cells.

32. (new) A communications system as claimed in claim 31, wherein the dynamic buffer queues the mini-cells in separate queues according to respective determined priorities of said mini-cells.

33. (new) A communications system as claimed in claim 29, wherein the packet scheduler processor is arranged to assemble said mini-cells into a CPS-PDU such that those mini-cells determined to have the highest priority are assembled first into the CPS-PDU.

34. (new) A communications system as claimed in claim 33, wherein, if all the mini-cells in the highest priority queue have been assembled into the CPS-PDU prior to expiry of the holdover timing period then the packet scheduler

processor assembles mini-cells from a queue of mini-cells having the next highest priority into said CPS-PDU.

35. (new) A communications system as claimed in claim 33, wherein, once the sustained inter-cell timing period (Tsus) has expired, the packet scheduler processor assembles minicells of any priority into the CPS-PDU.

36. (new) A method of dispatching ATM packets encapsulating real-time, delay sensitive traffic data on an ATM network connection, comprises the steps of:

scheduling assembly of said real-time, delay sensitive traffic data into ATM packets of an ATM bearer virtual circuit connection (VCC);

assembling said real-time, delay sensitive traffic data into the ATM packets of said bearer VCC under the control of a packet scheduler processor; and

controlling dispatch of the ATM packets in conformance with a traffic characteristic of said bearer VCC;

wherein said packet scheduler processor has a timer having a pre-set holdover timing period which is reset at the start of each ATM packet assembly process, whereby, if the holdover timing period expires prior to complete assembly of an ATM packet, then, on expiry of said holdover timing period, the packet scheduler dispatches the partially filled ATM packet.

37. (new) A method as claimed in claim 36, wherein it includes the step of resetting at the start of each ATM packet assembly process a minimum inter-cell timing period timer having a pre-set timing period (Tmin) whereby, if assembly of an ATM packet is completed prior to expiry of the inter-cell timing period, then the ATM packet is not dispatched until after expiry of said timing period (Tmin), and wherein said timing period (Tmin) is set such that it obeys the relationship:

Tmin ≤ holdover timing period.

38. (new) A method as claimed in claim 37, wherein the inter-cell timing period (Tmin) is set as the traffic characteristic of the bearer VCC.

39. (new) A method as claimed in claim 38, wherein the inter-cell timing period (Tmin) is a function of the permissible peak cell rate (PCR) of the bearer VCC.

40. (new) A method as claimed in claim 39, wherein the inter-cell timing period (Tmin) is set to be equal to the reciprocal of the PCR of the bearer VCC, namely Tmin = 1/PCR.

41. (new) A method as claimed in claim 37, wherein the traffic characteristic of the bearer VCC is set such that it is defined by both the minimum inter-cell timing period (Tmin) and a sustained inter-cell timing period (Tsus), where Tsus is a function of the permissible sustained cell rate (SCR) of the bearer VCC and where the sustained inter-cell timing period (Tsus) is set such that it obeys the relationship:

Tmin ≤ Tsus ≤ holdover timing period.

42. (new) A method as claimed in claim 41, wherein it includes, in addition to controlling dispatch of the ATM packets in conformance with a traffic characteristic of the bearer VCC defined by both the Tmin and Tsus timing periods, controlling dispatch of the ATM packets on said bearer VCC in accordance with a burst tolerance (BT) characteristic which is determined from the relationship:

BT = (MBS-1).(1/SCR-1/PCR)

where MBS is the maximum packet burst size permissible on the bearer VCC.

43. (new) A method as claimed in any one of claims 36 to 42, wherein it includes the step of multiplexing ATM common part sublayer payload data units (CPS-PDUs) assembled from ATM adaptation layer 2 mini-cells encapsulating the real-time, delay sensitive traffic data into the ATM packets for dispatch on the bearer VCC.

44. (new) A method as claimed in claim 43, wherein it includes the steps of receiving AAL2 mini-cells encapsulating said real-time, delay sensitive traffic data and determining an outgoing bearer VCC for each received mini-cell.

45. (new) A method as claimed in claim 44, wherein it includes the step of determining a priority for each received mini-cell.

46. (new) A method as claimed in claim 45, wherein it includes the step of queuing received mini-cells in separate queues in a dynamic buffer according to respective determined priorities of said mini-cells.

47. (new) A method as claimed in claim 43, wherein, where received mini-cells encapsulating the real-time, delay sensitive traffic data are determined to have different priorities, the method includes the steps of queuing said mini-cells in order of their determined priorities and assembling said mini-cells into a CPS-PDU such that those mini-cells determined to have the highest priority are assembled first into the CPS-PDU.

48. (new) A method as claimed in claim 47, wherein, if all the mini-cells in the highest priority queue have been assembled into the CPS-PDU prior to expiry of the holdover timing period then the method includes assembling mini-cells from a queue of mini-cells having the next highest priority into said CPS-PDU.

49. (new) A method as claimed in claim 47, wherein, once the sustained inter-cell timing period (Tsus) has expired, minicells of any priority are assembled into the CPS-PDU.

50. (new) A packet scheduler for an asynchronous transfer mode (ATM) communications system, comprising:

a packet scheduler processor for scheduling assembly of real-time, delay sensitive traffic data into ATM packets of an ATM bearer virtual circuit connection (VCC);

an assembly processor for assembling said real-time, delay sensitive traffic data into the ATM packets of said bearer VCC under the control of the packet scheduler processor; and

a control processor for controlling dispatch of the ATM packets in conformance with a traffic characteristic of said bearer VCC;

wherein said packet scheduler processor has a timer having a pre-set holdover timing period which is reset at the start of each ATM packet assembly process, whereby, if the holdover timing period expires prior to complete assembly of an ATM packet, then, on expiry of said holdover timing period, the packet scheduler dispatches the partially filled ATM packet.

51. (new) A packet scheduler as claimed in claim 50, wherein the packet scheduler processor has a minimum inter-cell period timer which has a pre-set timing period (Tmin) which is reset at the start of each ATM packet assembly process whereby, if assembly of an ATM packet is completed prior to expiry of the inter-cell timing period, then the packet scheduler does not dispatch said ATM packet until after expiry of said timing period (Tmin), and wherein said timing period (Tmin) is set such that it obeys the relationship:

$T_{min} \leq$ holdover timing period.

52. (new) A packet scheduler as claimed in claim 51, wherein the inter-cell timing period (Tmin) defines said traffic characteristic of the bearer VCC and is set to be equal to the reciprocal of the permissible peak cell rate (PCR) of the bearer VCC, namely Tmin = 1/PCR.

53. (new) A packet scheduler as claimed in claim 52, wherein the packet scheduler processor has a sustained inter-cell timing period timer having a pre-set time period (Tsus) which is set such that it obeys the relationship:

$T_{min} \leq T_{sus} \leq$ holdover timing period.

54. (new) A communications system as claimed in claim 53, wherein the Tsus and Tmin timing periods together define the traffic characteristic of the bearer VCC and wherein the Tsus timing period is set to be equal to the reciprocal of the permissible sustained call rate (SCR) of the bearer VCC, namely Tsus= 1/SCR.

55. (new) A packet scheduler as claimed in claim 54, wherein, in addition to controlling dispatch of the ATM packets in conformance with a traffic characteristic of the bearer VCC defined by both the Tmin and Tsus timing periods, the control processor is arranged to control dispatch of the ATM packets on said bearer VCC in accordance with a burst tolerance (BT) characteristic which is determined from the relationship:

$BT = (MBS-1).(1/SCR-1/PCR)$

where MBS is the maximum packet burst size permissible on the bearer VCC.

56. (new) A packet scheduler as claimed in any one of claims 50 to 55, wherein the assembly processor performs a multiplexing function to multiplex ATM common part sublayer payload data units (CPS-PDUs) assembled from

ATM adaptation layer 2 mini-cells encapsulating the real-time, delay sensitive traffic data into the ATM packets for dispatch on the bearer VCC.

57. (new) A packet scheduler as claimed in claim 56, wherein the packet scheduler includes an incoming packet processor for receiving the AAL2 mini-cells encapsulating said real-time, delay sensitive traffic data and for determining a priority for each received mini-cell and wherein said packet scheduler processor is arranged to assemble said mini-cells into a CPS-PDU such that those mini-cells determined to have the highest priority are assembled first into the CPS-PDU.

58. (new) A packet scheduler as claimed in claim 57, wherein, if all the mini-cells in the highest priority queue have been assembled into the CPS-PDU prior to expiry of the holdover timing period then the packet scheduler processor assembles mini-cells from a queue of mini-cells having the next highest priority into said CPS-PDU.

59. (new) A packet scheduler as claimed in claim 57, wherein, once the sustained inter-cell timing period (Tsus) has expired, the packet scheduler processor assembles minicells of any priority into the CPS-PDU.

60. (new) A method of operating a packet scheduler for dispatching ATM packets encapsulating real-time, delay sensitive traffic data on an ATM network connection, comprises the steps of:

scheduling assembly of real-time, delay sensitive traffic data into ATM packets of an ATM bearer virtual circuit connection (VCC);

assembling said real-time, delay sensitive traffic data into the ATM packets of said bearer VCC under the control of a packet scheduler processor; and

controlling dispatch of the ATM packets in conformance with a traffic characteristic of said bearer VCC;

wherein said packet scheduler processor has a timer having a pre-set holdover timing period which is reset at the start of each ATM packet assembly process, whereby, if the holdover timing period expires prior to complete assembly of an ATM packet, then, on expiry of said holdover timing period, the packet scheduler dispatches the partially filled ATM packet.

61. (new) A method as claimed in claim 60, wherein it includes the step of resetting at the start of each ATM packet assembly process a minimum inter-cell timing period timer having a pre-set timing period (Tmin) whereby, if assembly of an ATM packet is completed prior to expiry of the inter-cell timing period, then the ATM packet is not dispatched until after expiry of said timing period (Tmin), and wherein said timing period (Tmin) is set such that it obeys the relationship:

$T_{min} \leq$ holdover timing period.

62. (new) A method as claimed in claim 61, wherein the inter-cell timing period (Tmin) is set as the traffic characteristic of the bearer VCC is a function of the permissible peak cell rate (PCR) of the bearer VCC.

63. (new) A method as claimed in claim 61, wherein the traffic characteristic of the bearer VCC is set such that it is defined by both the minimum inter-cell timing period (Tmin) and a sustained inter-cell timing period (Tsus), where Tsus is a function of the permissible sustained cell rate (SCR) of the bearer VCC and where the sustained inter-cell timing period (Tsus) is set such that it obeys the relationship:

$T_{min} \leq T_{sus} \leq$ holdover timing period.

64. (new) A method as claimed in claim 63, wherein it includes, in addition to controlling dispatch of the ATM packets in conformance with a traffic

characteristic of the bearer VCC defined by both the Tmin and Tsus timing periods, controlling dispatch of the ATM packets on said bearer VCC in accordance with a burst tolerance (BT) characteristic which is determined from the relationship:

BT = (MBS-1).(1/SCR-1/PCR)

where MBS is the maximum packet burst size permissible on the bearer VCC.

65. (new) A method as claimed in any one of claims 60 to 64, wherein it includes the step of multiplexing ATM common part sublayer payload data units (CPS-PDUs) assembled from ATM adaptation layer 2 mini-cells encapsulating the real-time, delay sensitive traffic data into the ATM packets for dispatch on the bearer VCC.

66. (new) A method as claimed in claim 65, wherein, where received mini-cells encapsulating the real-time, delay sensitive traffic data are determined to have different priorities, the method includes the steps of queuing said mini-cells in order of their determined priorities and assembling said mini-cells into a CPS-PDU such that those mini-cells determined to have the highest priority are assembled first into the CPS-PDU.

67. (new) A method as claimed in claim 66, wherein, if all the mini-cells in the highest priority queue have been assembled into the CPS-PDU prior to expiry of the holdover timing period then the method includes assembling mini-cells from a queue of mini-cells having the next highest priority into said CPS-PDU.

68. (new) A method as claimed in claim 66, wherein, once the sustained inter-cell timing period (Tsus) has expired, minicells of any priority are assembled into the CPS-PDU.